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Comparative Analysis of Different Modulation Techniques For Five Level Diode Clamped Inverter With Boost Converter

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ABSTRACT
Now a days a Diode clamped inverter topologies are used as static VAR compensators, high voltage grid interconnections and variable speed motor drives. The objective of this paper is to balance DC link capacitor voltages and to test five level diode clamped inverter using different modulation techniques. In this paper capacitor voltage balancing is performed by a three level boost converter connected to the inner two capacitors and an additional balancing circuit is used to balance the other two capacitors and also five level diode clamped inverter is tested by using different pulse width modulation techniques. The results obtained from the MATLAB/SIMULINK is tabulated to compare the total Harmonic Distortion(THD) for different modulation techniques.
Key words: Five level Diode Clamped Inverter, Capacitor Voltage balancing, Three level boost converter, Modulation Index, Total Harmonic Distortion (THD).

I. INTRODUCTION

In recent years industries are demanding higher power devices operated at higher power levels. Today the connecting a single power semiconducting device to medium voltage grid is complicated. To address the above mentioned issue multilevel inverters is emerged as an important alternative in high power and medium voltage control. There are three multi level inverter topologies among them diode clamped inverter is extensively used by many researchers. The main advantage of multilevel inverter is to increase the power rating, lower harmonics and synthesized sinusoidal output waveform.

In [1], the effectiveness of various algorithms applied to a five level diode clamped inverter is discussed in terms of Total Harmonic Distortion (THD). Nabae and Takahashi [2] introduce design analysis and control of a neutral point clamped Pulse Width modulation inverter. He also discusses that the main problem in Diode Clamped Inverter is to balance the inner dc link capacitor voltage. Yuan and Barbi [3] propose a new diode clamped multilevel inverter in this new topology not only the main switches are clamped by the clamping diodes, the clamping diodes are also clamped mutually by themselves.

Peng et al [4] propose a new self balancing generalized multilevel topology. All the conventional diode clamped, capacitor clamped multilevel inverters are derived from this generalized topology. Chiasson and Knzie [5] designed a new control technique using resultant theory which can compute switching angle to produce required fundamental voltage. It also cancels out the higher order harmonics. Gui-Jia Su et al [6] present a new class of multilevel inverters with multilevel DC links and a bridge inverter to reduce the number of switches, clamping diodes, or capacitors.

Tolbert and Peng [7] propose a multilevel pulse width modulation technique with low modulation index. These novel carrier-based switching strategies can be used to enable better switch utilization in multilevel inverters. Holmes et al [8] present a general solution to various carrier based PWM methods for better harmonic cancellation.

This paper is organized as Section II gives the detailed explanation and operation of five level Diode clamped inverter. Section III discusses various types of carrier based modulation techniques. Section IV deals with the MATLAB/ Simulink results with the quantitative analysis by considering some of the performance evaluators. Finally Section V gives conclusion.

II. FIVE LEVEL DIODE CLAMPED INVERTER

The importance of multilevel inverters has been increased since last few decades. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum and with less Total Harmonic Distortion (THD). Numerous topologies have been introduced and widely studied for utility of non-conventional sources and also for drive applications. Amongst these topologies, the multilevel cascaded inverter was introduced in Static VAR compensation and in drive systems.

Diode-clamped multilevel inverters" use (m-1) clamped diodes and dc capacitors in order to generate ac voltage. This inverter is manufactured in 3, 4 and 5- level structures. A typical five level inverter topology is shown in Figure 1. Here for each leg there are four positive thyristors and four negative thyristors. These positive and negative thyristors are controlled using a opposite polarity PWM signal.

Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg A are (Sa1, Sa'1), (Sa2, Sa'2), (Sa3, Sa'3), and (Sa4, Sa'4). Table 1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg is always adjacent and in series.

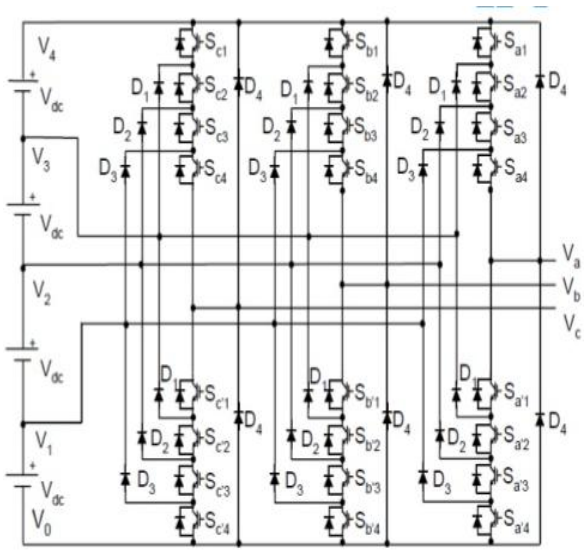

Fig. 1 Schematic diagram for five level diode clamped inverter (FLDCI)

TABLE 1 VOLTAGE LEVELS AND SWITCHING STATES FOR FLDCI

Voltage V_0	SWITCH STATE							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a1}	S'_{a2}	S'_{a3}	S'_{a4}
$V_4 = 4V_{dc}$	1	1	1	1	0	0	0	0
$V_3 = 3V_{dc}$	0	1	1	1	1	0	0	0
$V_2 = 2V_{dc}$	0	0	1	1	1	1	0	0
$V_1 = V_{dc}$	0	0	0	1	1	1	1	0
$V_0 = 0$	0	0	0	0	1	1	1	1

The following are the some advantages and disadvantages of the DCMLI:

Advantages: -

1. As the number of levels increases the harmonic content of the output waveform decreases the filter size.
2. Lower switching losses due to the devices being switched at the fundamental frequency without increasing the harmonic content in the output.
3. Reactive power flow can be controlled, as this does not cause unbalance in the capacitor voltages.
4. Fast dynamic response.
5. Back to back operation is possible.

Disadvantages: -

1. High number of clamping diodes is required as the number of levels increase.
2. Active power transfer causes unbalance in the DC bus capacitors, this complicates the control of the system.

Fig. 2 shows one of the three line-line voltage waveforms for a five-level DCMLI. The line voltage Vab consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is a 9-level staircase waveform. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a (2m-1)-level output line voltage.

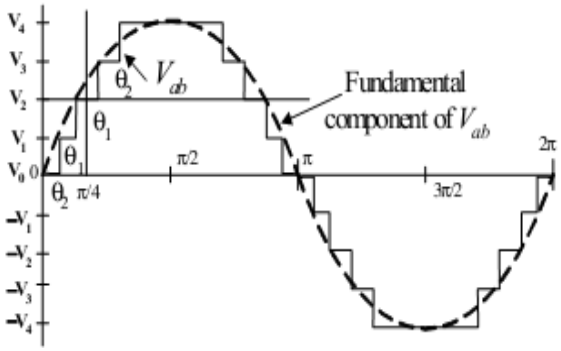

Fig. 2 Line voltage wave form for FLDCI

III. TYPES OF CARRIER BASED MODULATION TECHNIQUES

According to the carrier and the modulating signal Sinusoidal PWM is classified into various types. They are given as below.

A. Phase Opposition Disposition (POD) PWM

To construct a phase opposition disposition PWM for multilevel inverter the step by step procedure is as follows

- The carrier waveforms are arranged as shown in figure 3. The total number of carriers should be (m-1) where m is the number of levels.
- Now the converter is operated at a voltage level of +Vdc/2 when the reference sine wave is greater than the upper two carrier waveforms.
- The converter is operated at a voltage level of +Vdc/4 when the sine reference is greater than the first upper carrier.
- The converter is operated at a voltage level of Zero when the sine wave is lower than upper carrier but higher than lower carrier.
- The converter is operated at a voltage level of -Vdc/4 when the sine reference is lower than the first lower carrier
- The converter is operated at a voltage level of -Vdc/2 when the sine reference is lower than both lower carriers.

The above procedure is similar for all other modulation techniques rather than the arrangement of the carriers.

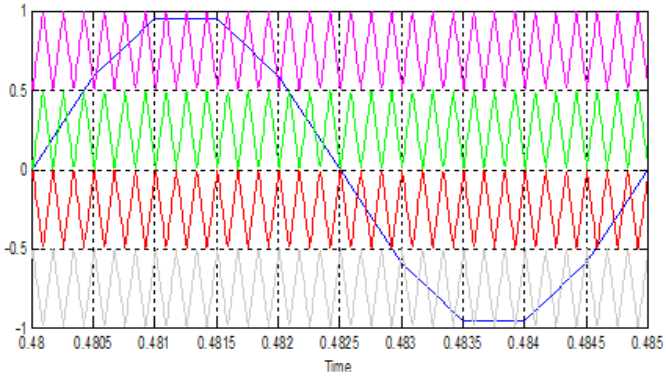

Fig. 3 Carrier and reference wave arrangement for PODPWM

B. Phase Disposition (PD) PWM

In this technique the carriers are arranged in phase to each other as shown in figure 4

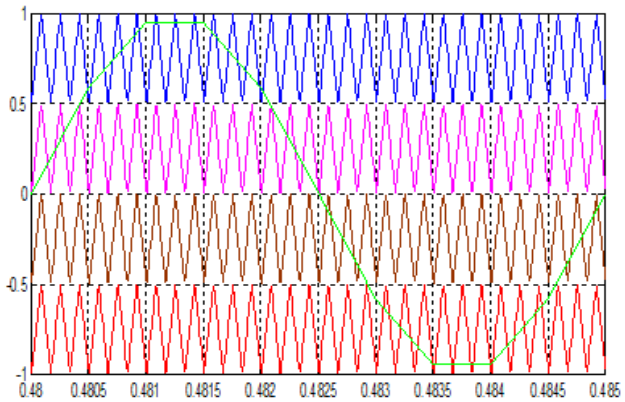

Fig. 4 carrier arrangement for PDPWM

C. Alternative Phase Opposition Disposition (APOD) PWM

In this technique all the (m-1) carriers required to get the m level output should displaced and 180^0 phase shift with each other alternatively. The arrangement of carriers is shown in figure 5

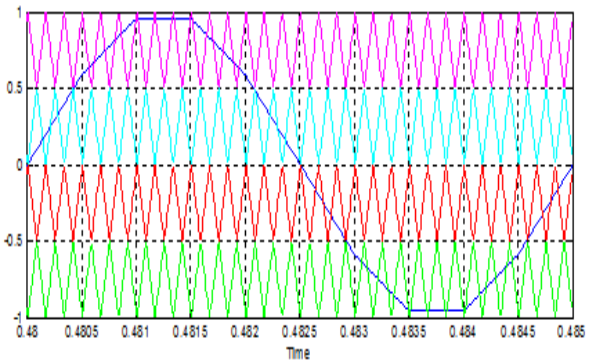

Fig. 5 Carrier arrangement for APODPWM

D. Carrier Overlapping (CO) PWM

In this technique all the m-1 carriers are arranged such a way that some portion of each carrier will overlap with the neighboring carrier. The arrangement along with the reference wave is shown in figure 6

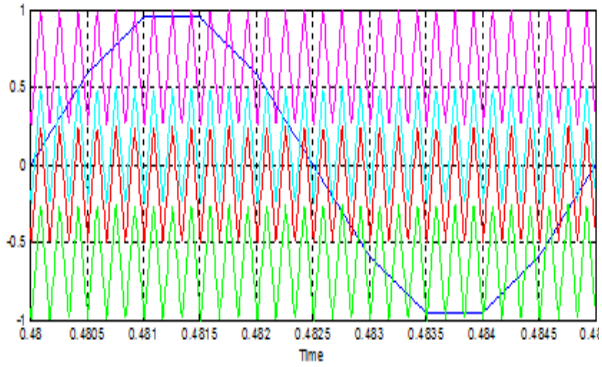

Fig. 6 Carrier arrangement for COPWM

E. Phase Shifting (PS) PWM

In this technique all the m-1 carriers are displaced such a way that they have a phase shift of 0^0, 90^0, 180^0, and 270^0 respectively. The carrier arrangement along with the sinusoidal reference is shown in figure 7

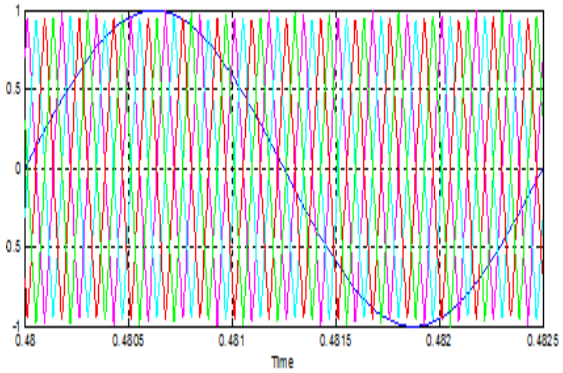

Fig. 7 Carrier arrangement for PSPWM

F. Inverted Sine (IS) PWM

In this technique all the m-1 carriers are taken as inverted sine wave with equal magnitude and are displaced as like in PDPWM technique. The arrangement of carriers is shown in figure 8

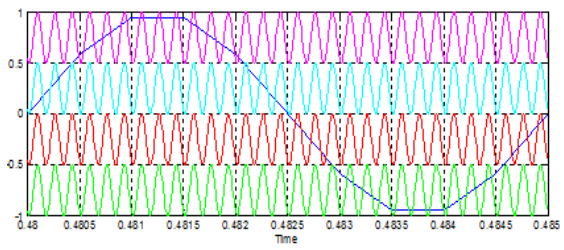

Fig. 8 Carrier arrangement for ISPWM

G. Variable Frequency (VF) PWM

In this technique all the m-1 carriers are arranged such a way that first and last carrier will have double the frequency when compared with the middle two carriers. The arrangement of carriers is shown in figure 9.

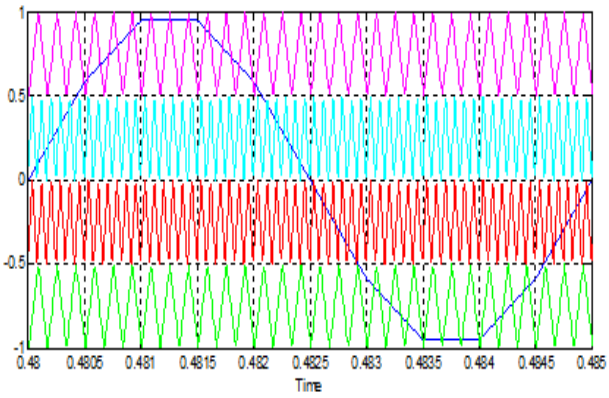

Fig. 9 Carrier arrangement for VFPWM

IV. MATLAB/ SIMULINK RESULTS AND DISCUSSION

In this paper a five level diode clamped inverter is modeled using MATLAB/ Simulink along with the three level boost converter to balance the dc link capacitors. Here a separate technique is employed to control the inner dc link capacitors and outer dc link capacitors.

The inner two capacitors are controlled using a three level boost converter and the outer two capacitors are controlled using generalized method by taking the voltage across inner capacitors as reference. The detailed MATLAB/ Simulink model for a Three phase five level diode clamped inverter with three level boost circuit is shown in figure 10.

Simulation studies are performed by using MATLAB/SIMULINK to verify the proposed multi carrier based PWM strategies for three phase five level diode clamped inverter with three level boost circuit for various values of ma ranging from 0.6 – 1 and corresponding %THD values are measured using FFT block and they are shown in Table 2. Table 3 shows the VRMS of fundamental of inverter output for the same modulation indices.

Figs.11-22 show the simulated output voltages, currents of chosen FCMLI and the corresponding FFT plots with different strategies but only for one sample. Fig.11 shows the five level output voltage, current generated by PDPWM strategy and its FFT plot is shown in Fig.12. By observing the THD wave forms of different

modulation techniques in Fig. 20 the ISPWM produce significant energy for 7^{th}, 9^{th}, 11^{th}, 13^{th} harmonics.

The following parameter values are used for simulation: VIN=165V, fc=6000Hz and R (load) =150 ohms

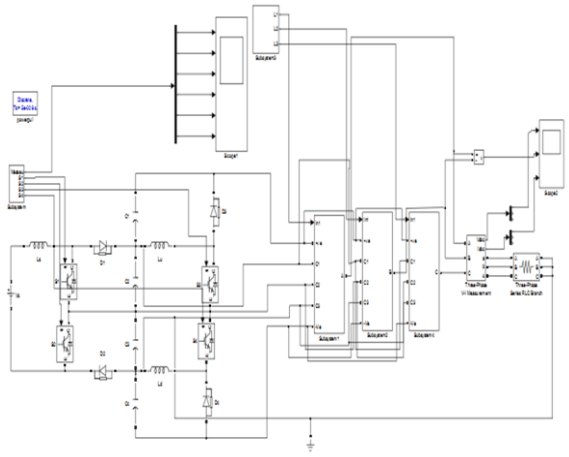

Fig. 10 Detailed MATLAB/ Simulink model for three phase FLDCI using three level boost circuit

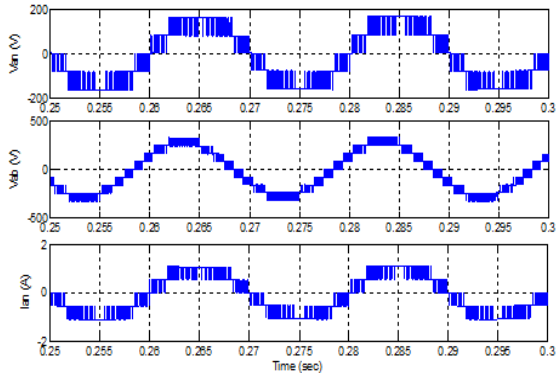

Fig. 11 output voltage and current wave forms for PDPWM

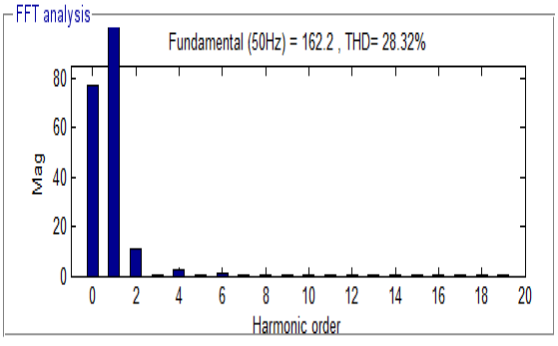

Fig. 12 % THD for PDPWM

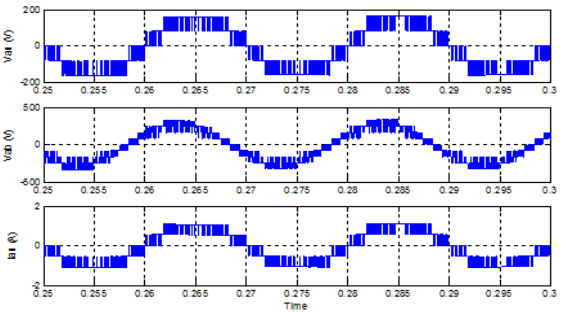

Fig. 13 output voltage and current waveforms for PODPWM

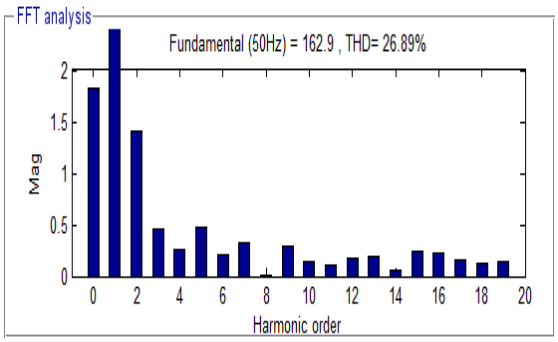

Fig.14 % THD for PODPWM

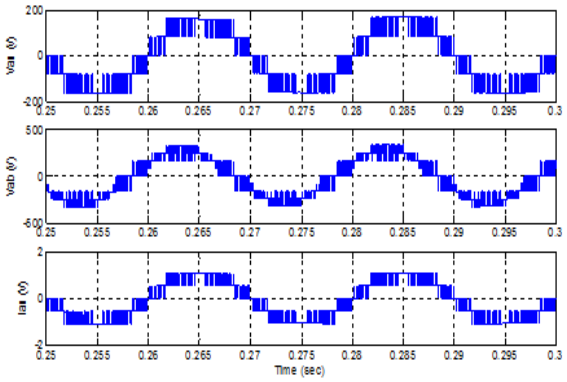

Fig. 15 output voltage and current waveform for APODPWM

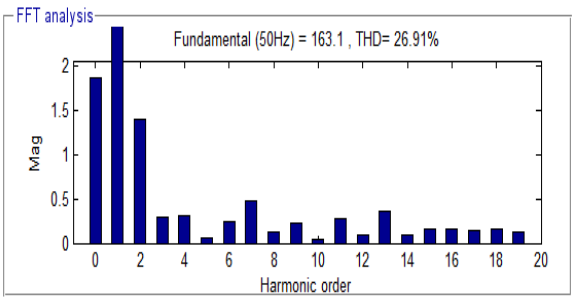

Fig. 16 %THD for APODPWM

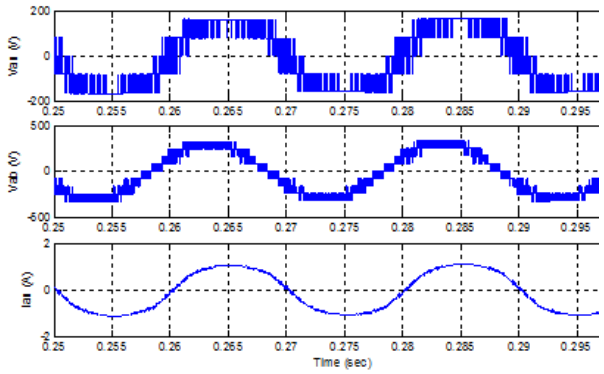

Fig. 17 output voltage and current waveforms for COPWM

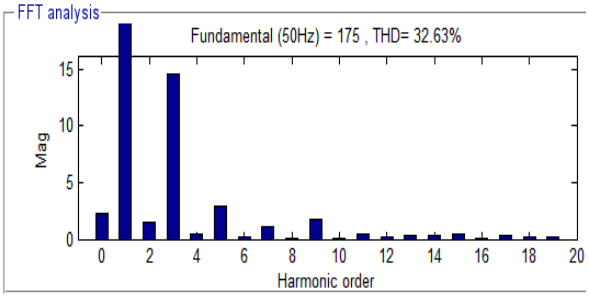

Fig. 18 % THD for COPWM

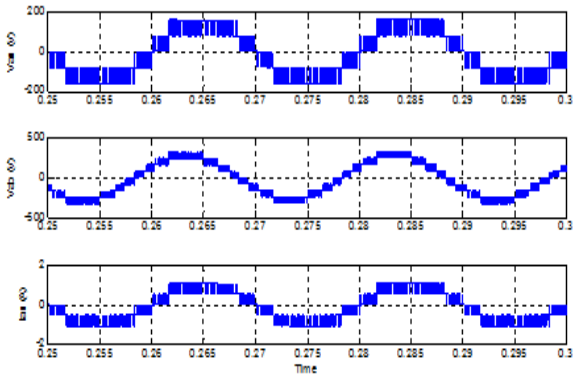

Fig. 19 output voltage and current waveforms for ISPWM

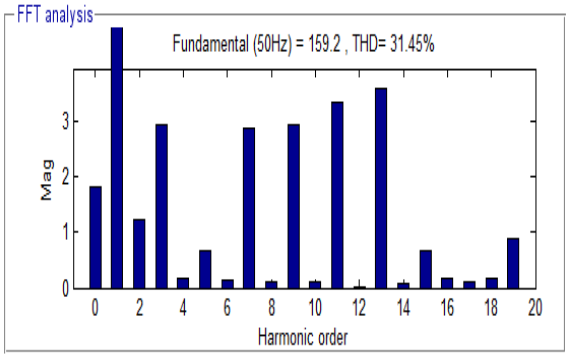

Fig. 20 % THD for ISPWM

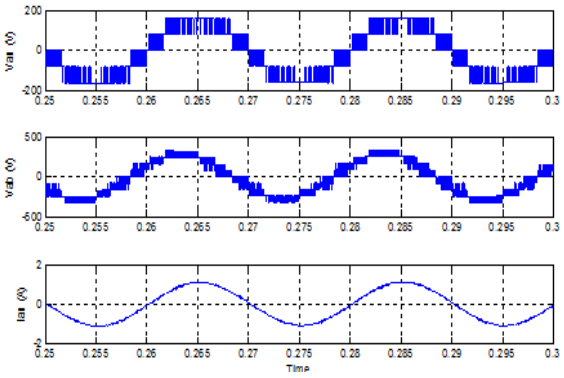

Fig. 21 output voltage and current waveform for VFPWM

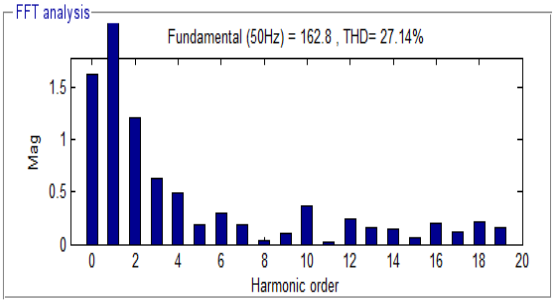

Fig. 22 % THD for VFPWM

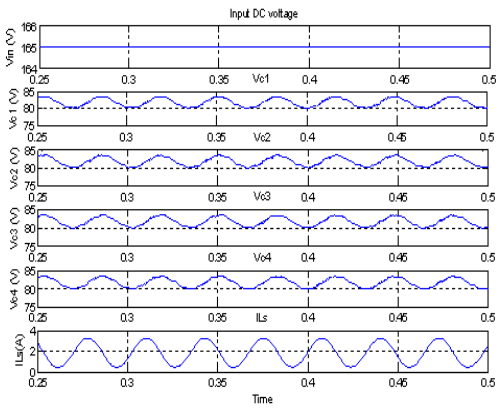

Fig. 23 Input DC voltage, Capacitor voltages and Inductor current waveforms

Tables 4 and 5 gives the Form Factor (FF) and Crest Factor (CF) corresponding to the output wave for m for three phase five level diode clamped inverter with three level boost circuit.

TABLE 2 % TOTAL HARMONIC DISTORTION (% THD)

ma	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM	IS PWM
1	27.09	26.96	27.07	32.35	26.95	31.40
0.9	33.63	33.55	33.66	37.49	33.57	37.51
0.8	38.52	38.47	38.5	42.5	38.24	41.3
0.7	41.86	41.84	41.84	47.39	41.98	45.14
0.6	44.36	44.37	44.49	53.53	44.20	50.08

TABLE 3 OUTPUT VOLTAGE (V_{RMS})

ma	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM	IS PWM
1	116.7	116.7	116.8	125.8	116.5	114
0.9	104.6	104.7	104.5	117.2	104.4	102.7
0.8	92.52	92.55	92.53	108.2	92.37	93.2
0.7	80.67	80.58	80.64	99.07	80.78	83.26
0.6	68.87	68.72	69.03	89.13	68.88	71.54

TABLE 4 FORM FACTOR (FF)

ma	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM	IS PWM
1	1.11	1.11	1.11	1.11	1.11	1.11
0.9	1.11	0.981	1.11	1.11	1.11	1.11
0.8	1.11	1.11	1.11	1.11	1.11	1.11
0.7	1.11	1.11	1.11	1.11	1.11	1.11
0.6	1.11	1.11	1.11	1.11	1.11	1.11

TABLE 5 CREST FACTOR (CF)

ma	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM	IS PWM
1	1.413	1.413	1.413	1.414	1.414	1.414
0.9	1.413	1.414	1.414	1.414	1.414	1.413
0.8	1.413	1.414	1.414	1.414	1.413	1.414
0.7	1.414	1.414	1.413	1.414	1.413	1.414
0.6	1.414	1.414	1.414	1.413	1.414	1.414

V. CONCLUSION

A three phase five level Diode Clamped inverter with three level boost circuit is employed and the performance indices are calculated for various modulation techniques with a single reference waveform. From all the comparisons it is observed that the inverter with VFPWM will have lower harmonic factor for all modulation index. The inverter with COPWM is performed better in terms of getting greater fundamental RMS output voltage when compared to the other techniques.

In the near future the work can be extended as follows:

1. Three phase five level inverter can be extended to operate for multiple numbers of phases which can facilitate to run the drive system with higher order motors.
2. The dc link capacitors of a Three phase five level inverter can be balanced by using advanced techniques.

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